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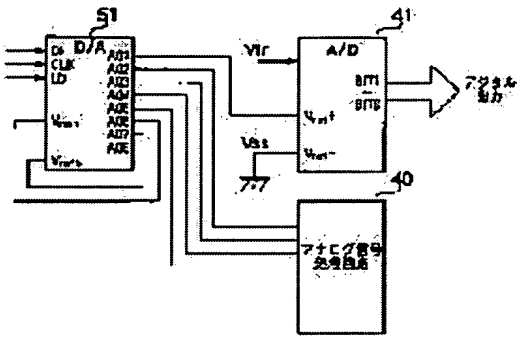
(54) IMAGE READER

(57)Abstract:
PROBLEM TO BE SOLVED: To stably obtain a read image with high image quality by allowing a D/A converter setting a conversion use reference signal (conversion parameter) to adjust the setting value at a maximum dynamic range in the case of digitizing an image signal from an image sensor so as to enhance digital conversion accuracy and accuracy of various level correction of the image signal conducted at the same time with this adjustment.
SOLUTION: A setting value outputted from a D/A converter 51 is used for offset and gain adjustment for an analog signal processing circuit 40 processing an image signal and for reference signal adjustment of an A/D convert 41. The D/A converter 51 to which a fed back digital output from the A/D converter 41 is inputted as a DI outputs setting values from A01-A05 on the basis of reference voltages Vreft, Vrefb that can be adjusted externally. The reference voltages Vreft, Vrefb are set again on the basis of a maximum value and a minimum value of the output of the A/D converter 41 obtained by correcting various levels by using the reference voltages Vreft, Vrefb for the initial values to adjust the setting values at the maximum dynamic range.



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CLAIMS

[Claim(s)]
[Claim 1]An image sensor.
A picture signal processing means to process and change an analog picture signal outputted from this image sensor based on parameter value set as variable.
A control means which controls operation of this picture signal processing means.
It is the image reader provided with the above, and said control means adjusts parameter value which a dynamic range equips with a controllable D/A converter and to which it is set by this D/A converter in said picture signal processing means.

[Claim 2]While said picture signal processing means has an A/D converter which carries out the A/D conversion of the analog picture signal outputted from said image sensor based on a reference signal value set as variable, The image reader according to claim 1, wherein a preset value of a reference signal in this A/D converter is adjusted by said D/A converter.
[Claim 3]While said picture signal processing means has an analog signal processing circuit which processes an analog picture signal outputted from said image sensor based on a processing parameter set as variable, The image reader according to claim 1 or 2, wherein a preset value of a processing parameter in this analog signal processing circuit is adjusted by said D/A converter.

[Claim 4]An image reader given in two to either of claims 1 thru/or 3, wherein a dynamic range is controlled based on a digital output to which said D/A converter is outputted from said A/D converter.
[Claim 5]The image reader according to any one of claims 1 to 4 performing control of a dynamic range of said D/A converter by adjusting a preset value of a reference signal used for D/A conversion.
[Claim 6]The image reader according to any one of claims 2 to 5, wherein said D/A converter performs gray balance amendment of a picture signal by adjusting a preset value of a reference signal in said A/D converter based on the output.
[Claim 7]The image reader according to any one of claims 3 to 6, wherein said D/A converter performs black level correction of a picture signal, and/or white level amendment by adjusting a preset value of a processing parameter in said analog signal processing circuit based on the output.

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DETAILED DESCRIPTION

[Detailed Description of the Invention]
[0001]
[Field of the Invention]In this invention, the level of the reference signal used for the analog processing of the picture signal output from a line image sensor and A/D conversion processing is adjusted more to details about the image reader which reads a manuscript by the scan of a line image sensor according to a sensor output.
Therefore, it is related with the image reader which raised the accuracy of the picture signal output after processing.

[0002]
[Description of the Prior Art]It is ********** about amendment of the shading compensation etc. which amend the luminous energy distribution of a light source, and the sensitivity distribution of CCD to the picture signal which performed the image input with the line image sensor (CCD) of the image reader, and was read in the former by CCD in a copying machine, a scanner, etc. Since these processings are usually performed in the stage which digitized after carrying out the A/D conversion of the analog output from CCD in the case of a digital machine, the fall of resolution is not avoided for a quantization error. Also when carrying out an A/D conversion, taking offset used as the factor which lowers resolution, and changing a profit into the optimal possible state and carrying out an A/D conversion, it is necessary to remove the influence of the ground of a manuscript and to make a picture output with the digital value of a high resolution (high gradation), in order to cope with such a thing.
[0003]one conventional example proposed as art to which the picture which should remove and read the influence of the ground of a manuscript is made to output with the digital value of a high resolution is because the reference voltage of an A/D converter is changed. When this changes fixed voltage and a programmed voltage for the reference voltage of an A/D converter with a switch and it reads only one manuscript, A switch chooses fixed voltage, and when reading the manuscript conveyed one by one by an automatic draft feeder in a read position, a switch chooses the variable voltage set up by analog circuitry composition, is changed according to a generating picture, and enables it to adjust image concentration automatically properly.
[0004]One example which will be accepted is what performs an automatic setup of the reference signal for A/D conversions by a different method from the above conventionally, The peak hold circuit which detects the peak value of the output from an A/D converter is provided, the reference signal for A/D conversions is controlled and the high-resolution digital output of the picture which should be read is secured so that the peak value detected by this circuit may serve as a full scale of an A/D conversion. Therefore, in this example, after processing the digital output from an A/D converter by a digital circuit system, the D/A converter was provided in the final stage, it changed into the analog value, and this is inputted into the A/D converter as a reference signal for A/D conversions. Operation of the A/D converter at the time of adjusting the reference signal of the A/D converter performed to this appearance and a D/A converter is explained more below at details.
[0005]Drawing 8 is a figure showing the outline composition of an A/D converter. A/D converter

41 like a graphic display The one analog input terminal Vin, The digital output terminals BIT0-BIT7 for two or more minutes (for example, 8 bits), It has terminal $Vref^+$ for maximums (the power supply voltage VCC is taken as the maximum), and terminal $Vref^-$ for minimums (ground voltage VSS is usually taken) as the clock terminal CLK which determines the timing of an A/D conversion, and a terminal which determines the reference voltage of the upper and lower sides for A/D conversions. Total of the digital output from A/D converter 41 : sigmaBITi, If it is decided by Vin, $Vref^+$, and $Vref^-$ and a full scale of a digital output is set to FS, it will be $sigmaBITi=FSx(Vin-Vref^-)/(Vref^+-Vref^-)$.... (1)
If it carries out, and it is expressed and $Vref^-$ is made into a ground with resolution (i= 8) of 8 bits, since it will be $Vref^-=0$ and FS=255, the above-mentioned formula (1) is $sigmaBITi=255xVin/Vref^+$.... (2)
It becomes. That is, total of a digital output is determined by the ratio of Vin and $Vref^+$. reference voltage -- upper limit -- the digital output by Vin in that case if setting out of the pressure value of $Vref^+$ is lower than Vin -- a full scale -- 255 will be outputted, but to Vin, if too high, gradation will be made useless. Therefore, as for the value of $Vref^+$, it is desirable to set up become equal to the maximum which Vin can take. In order to set this up automatically, the analog value according to a peak value is set up as $Vref^+$ by performing the peak hold of the digital output of A/D converter 41, and inputting the held peak value into a D/A converter.
[0006]Drawing 9 is a figure showing the outline composition of a D/A converter. The input terminal Vreft in which D/A converter 51 leads to the power supply VCC like a graphic display. everything but the input terminal Vrefb connected with grand VSS -- serial-data input terminal DI, the shift clock input terminal CLK, LD input terminal, and two or more minutes -- for example, the analog output terminals A01-A08 of ** are formed by eight channels. Since part precision, temporality, environment, etc. may become a factor and dispersion may arise, the voltage VCC of constant value has been built over the terminal Vreft for maximums.
It is usually made into VCC=5(V).
The serial data whose data length is 12 bits are inputted into serial-data input terminal DI. As for 8 bits of low ranks of serial data, top 4 bits becomes address selections by the object for level setting of output voltage. The input signal from DI input terminal is inputted into 12 bit shift registers in the standup of the shift clock inputted from the shift clock input terminal CLK. If a High level is inputted into LD input terminal, the value of the data currently held at 12 bit-shift REJITA will be set in the register for an output. In the circuitry of this conventional example, by 5(V), supposing Vrefb is 0(V) in GND, Vref in the above-mentioned formula (2) will serve as 5(V) s, and as for Vin, Vreft which takes the fixed pressure value is digitized at a rate over 5(V)s. Therefore, the voltage per data 1 step becomes 5(mV) / 255 (mV), i.e., about 20.
[0007]
[Problem(s) to be Solved by the Invention]However, in adjustment of the above-mentioned reference voltage of an A/D converter, like the first example, when reference voltage is set up by the system of analog circuitry composition, a system is in instability, and it is **. For example, when the noise which has especially a constant period on a pulse when a noise mixes in a power supply mixes, a noise depressing effect with an amplifier will decrease remarkably, and a noise will mix also in an output. Since a peak hold or sample hold has determined the reference voltage level for A/D converters in the unstable state where ** which a noise will mix also according to ambient conditions, and such a noise can mix, it becomes a thing in which the stability of the whole system is also spoiled. Since the level fluctuation by temperature may arise, image deterioration will arise gradually over a long time. If the accuracy of amendment was also required and the reference signal Vref of the D/A converter was fixed to constant value (5(V)) in the second example when high definition was required, It becomes impossible for the dynamic range of a D/A converter to be insufficient, it cannot adjust to the value of a request of the reference voltage set as an A/D converter, and cannot meet the high-definition demand enough.

[0008]This invention was made in view of the problem of the above conventional technologies, and the purpose, When digitizing the analog picture signal from an image sensor, the D/A converter which sets up the reference signal (processing and conversion parameter) used for processing and conversion of a picture signal is made to adjust a preset value with the greatest dynamic range, It is in providing the reader which makes it possible to obtain a high-definition read picture by being stabilized by raising the accuracy of various level adjusting of a picture signal performed by raising the accuracy of the digital conversion of a picture signal, and adjusting processing and a conversion parameter simultaneously.
[0009]
[Means for Solving the Problem]A picture signal processing means by which an invention of claim 1 processes and changes an analog picture signal with which it is outputted from an image sensor and this image sensor based on parameter value set as variable, In an image reader which it has, a control means which controls operation of this picture signal processing means said control means, A dynamic range is provided with a controllable D/A converter, and constitutes an image reader adjusting parameter value set up by this D/A converter in said picture signal processing means.
[0010]In the image reader according to claim 1, an invention of claim 2 said picture signal processing means, While having an A/D converter which carries out the A/D conversion of the analog picture signal outputted from said image sensor based on a reference signal value set as variable, A preset value of a reference signal in this A/D converter is adjusted by said D/A converter.
[0011]In the image reader according to claim 1 or 2, an invention of claim 3 said picture signal processing means, While having an analog signal processing circuit which processes an analog picture signal outputted from said image sensor based on a processing parameter set as variable, A preset value of a processing parameter in this analog signal processing circuit is adjusted by said D/A converter.
[0012]As for an invention of claim 4, in the image reader according to any one of claims 1 to 3, a dynamic range is controlled based on a digital output to which said D/A converter is outputted from said A/D converter.
[0013]An invention of claim 5 performs control of a dynamic range of said D/A converter by adjusting a preset value of a reference signal used for D/A conversion in the image reader according to any one of claims 1 to 4.
[0014]In the image reader according to any one of claims 2 to 5, an invention of claim 6 performs gray balance amendment of a picture signal, when said D/A converter adjusts a preset value of a reference signal in said A/D converter based on the output.
[0015]In the image reader according to any one of claims 3 to 6, an invention of claim 7 said D/A converter, By adjusting a preset value of a processing parameter in said analog signal processing circuit based on the output, black level correction of a picture signal and/or white level amendment are performed.
[0016]
[Embodiment of the Invention]It explains based on the example of the following shown with the drawing which attaches this invention. Drawing 1 is a figure showing the outline of the composition of the color copy reader which applied this invention. First, the entire configuration of this device is explained with reference to drawing 1. The contact glass 1 with which a device lays the manuscript 14, and the halogen lamp 2 for manuscript exposure, The 1st carriage 6 in which the 1st reflective mirror 3 was laid, and the 2nd carriage 7 in which the 2nd reflective mirror 4 and the 3rd reflective mirror 5 were laid, Three-line type color CCD series 9 which carries out photoelectric conversion of the picture in which image formation is carried out by the lens unit 8, It comprises the sensor board board 10, the CCD signal treating substrate 12 which performs various kinds of processings to a picture signal, the connecting cable 11, the white reference board 15 for amending various kinds of distortion by a reading light study system etc., and the scanner body 13 that equips these. At the time of reading operation, with a stepping motor (not shown), it is moved in the direction of arrow A in a figure, and the 1st carriage 6 and the 2nd carriage 7 carry out vertical scanning of the manuscript surface on the contact glass 1,

and read the whole manuscript surface.
[0017]Drawing 2 is a figure showing the acceptance surface of three-line type color CCD series 9. Reduced type CCD which coated the filter of each color of the decomposed colors R (red), G (green), and B (blue) as each line image sensor by the type which was able to be located in a line. As for R-CCD16, G-CCD17, and B-CCD18, the dot position of the scanning direction is the same the arrangement which shifted to the vertical scanning direction A the constant interval every. Therefore, since each color outputs have delay in the vertical scanning direction A, the amendment using a line memory is needed. Drawing 3 is a block diagram showing the circuitry of three-line type color CCD series 9. It has a register of two rows which R-CCD16, G-CCD17, and B-CCD18 divide the picture signal detected by the even number (EVEN) pixel and odd number (ODD) pixel in each light sensing portion, and holds each signal. The picture signal VRE, VRO, VGE, VGO, VBE, and VBO are independently outputted by driving a register synchronizing with (that is, on the whole, it has CCD registers 1-6) and a drive pulse.
[0018]Drawing 4 is a time chart which shows the correlation of the timing of various kinds of signals for driving CCD. The shift signal SH for transporting to a CCD register from a light sensing portion, and the transfer clock phi 1 for carrying out charge transfer of the inside of a CCD register and phi 2, A drive pulse generally comprises phiCLP for clamping pulse phiRS for resetting the output buffer in CCD, and the electric black level immediately after reset. Receiving light is continued during the period when a light sensing portion is from the shift signal SH to the following shift signal SH. This time is called storage time. The transfer clock phi 1 and phi 2 are the frequency which can transmit all the pixels of CCD in this storage time, and it becomes conditions that a transfer clock does not move during active period length in the shift signal SH. Vo shown in drawing 4 is a generating picture. Drawing 5 is a block diagram showing more in details the image processing circuit which it has in the signal processing substrate 12 in the color copy reader of drawing 1. The signal processing substrate 12 is equipped with the analog signal processing circuit 40, the A/D conversion circuit 41, the shading correction circuit 42, the correction circuit 43 between lines, the control circuit 44, and the oscillator 45.
[0019]Operation of an image processing circuit is mainly explained with reference to drawing 5. First, it is irradiated with a manuscript by the halogen lamp 2, and reduction image formation of the catoptric light from the manuscript 14 is carried out on three-line type color CCD line sensor 9 through the lens unit 8 through the 1st carriage 6 and the 2nd carriage 7, and it is read for every line. On the sensor board board 10 which receives the read picture signal, a picture signal is outputted to the CCD signal treating substrate 12 from three-line type color CCD line sensor 9 synchronizing with the drive pulse SH. This analog picture signal is inputted into the analog signal processing circuit 40 of the CCD signal treating substrate 12. By sampling a picture signal by a sample pulse, respectively, and holding it by a sample hold circuit (not shown), in the analog signal processing circuit 40, A picture signal is made into the continuous analog signal, the level of the dark output of CCD is detected in a black level correction circuit (not shown), the variation in a signal is amended on the basis of a black level, and the picture signal after amendment is outputted. In order that a picture signal may amend the real light volume decided by relation between CCD sensitivity and manuscript surface illumination, AGC (Auto Gain Control) is made.
[0020]The analog signal outputted from the analog signal processing circuit 40 is changed into a digital signal by the A/D conversion circuit 41. It is carried out by digital processing after the shading correction circuit 42 of the next step, and here, Based on the picture signal which read the catoptric light of the white reference board 15 irradiated by the halogen lamp 2 with three-line type color CCD line sensor 9, the luminous-intensity-distribution nonuniformity of the variation in the sensitivity of CCD or illuminating system is amended so that the level of predetermined concentration may be obtained. In the correction circuit 43 between lines, a gap of each line is amended using the memory for amendment between lines, and the delay produced between R [of a vertical scanning direction], G, and B each line writing with 3line type as explained with reference to drawing 2 is outputted as a picture signal read in the same position. In the control circuit 44, the control signal which controls operation of each above-mentioned processing circuit 40, i.e., an analog signal processing circuit, the A/D conversion circuit 41, the

shading correction circuit 42, and the correction circuit 43 between lines is generated. in addition -- being based on the clock from the oscillator 45 in that case -- a system -- the whole operation and the timing of a signal are adjusted.
[0021]In the CCD signal treating substrate 12, from three-line type color CCD line sensor 9 to R. G and B -- about each the two analog picture signals (ODD, EVEN) VRE, VRO, VGE, VGO, VBE, and VBO in the analog processing circuit 40, [amend and] It is necessary to change into a digital value by A/D converter 41 of the next step, it is necessary to perform initial setting so that reading operation of the scanner part which actually reads a manuscript can be performed, and control for it is performed. In this case, by A/D converter 41, gray balance amendment (Vref adjustment) is performed for ODD/EVEN difference amendment, black level correction (DC offset amendment), and white level amendment (gain control) in the analog signal processing circuit 40. In this invention, these amendments are performed based on the digital output value of A/D converter 41, and it is controlled by the analog value outputted from the D/A converter which considers this digital value as an input. He is trying to adjust the reference voltage in a D/A converter to the greatest dynamic range by feeding back the digital output of A/D converter 41. Feedback of the digital output value in this control is performed when CPU (not shown) of the control circuit 44 reads the data currently held with the digital value detection register of the shading correction circuit 42. The input to a D/A converter is performed via the control circuit 44 in the form of 12 bits (8 bits of data) serial data.
[0022]Next, the initialization action in each processing circuit by the composition of a control system and the control system which consist of the analog signal processing circuit 40 and A/D converter 41 which are controlled by a D/A converter and the D/A converter is explained in detail. Drawing 6 is a block diagram showing the composition of this control system. A control system consists of D/A converter 51 into which control data is inputted with a digital value, A/D converter 41 by which the analog output from D/A converter 51 is set up, and an output is controlled with the set-up value, and the analog signal processing circuit 40. Serial-data input terminal DI, the shift clock input terminal CLK, LD input terminal, and the analog output terminals A01-A08 for eight channels other than the input terminals Vreft and Vrefb of reference voltage with which D/A converter 51 can adjust voltage from the exterior are provided. The serial data whose data length is 12 bits are inputted into serial-data input terminal DI. As for 8 bits of low ranks of serial data, top 4 bits becomes address selections by the object for level setting of output voltage. The input signal from DI input terminal is inputted into 12 bit shift registers in the standup of the shift clock inputted from the shift clock input terminal CLK. If a High level is inputted into LD input terminal, the value of the data currently held at 12 bit-shift REJITA will be set in the register for an output. The output voltage Vout of D/A converter 51 will change by the reference voltage Vreft and Vrefb which can be adjusted from input data: <DATA> and the outside, and the relation becomes like the following formulas.
Vout=Vrefb+(Vreft-Vrefb) x<DATA>/255 [0023]Drawing 7 shows the flow chart of the initialization action of each processing circuit performed by the above-mentioned control system. With reference to drawing 7, an initialization action is explained below. It writes in addition by parenthesis writing into an explanatory note for reference of the step number of drawing 7. At the time of the start of initial setting, an initial value is set as the reference voltage Vreft and Vrefb of D/A converter 51 (S1). Here, it is considered as Vreft=5(V) and Vrefb=0(V). When taking the composition of drawing 6, this reference voltage is made possible by setting out by setting <DATA> =0 as the channel of the analog output terminal A06 at the channel of <DATA>=255 and A07. The voltage per step at this time becomes (5-0) / 255(V), and is set to about 20 (mV).
[0024]By adjusting the output from the output terminals A02 and A03, and setting that value as the analog signal processing circuit 40 on this condition, Black level correction (DC offset amendment) is performed (S2), the output from the output terminals A04 and A05 is adjusted, and white level amendment (gain control) is performed with the value (S3). Gray balance amendment (Vref adjustment) is performed by adjusting the output from the output terminal A01, and setting the value as $Vref^+$ of A/D converter 41. Next, the maximum obtained as a procedure

adjusted to the greatest dynamic range by A01-A05 which were set up with the input value <DATA>, The minimum is calculated, the value exceeding a little maximum is set as the output terminal A06 (Vreft), and a value somewhat smaller than the minimum is reset to the output terminal A07 (Vrefb) (S5). The maximum of <DATA> concerning setting out to A01-A05 here, for example 200 (about 3.92 (V)s), When the minimum is 100 (about 1.96 (V)s), Vreft=4.0(V) of the output terminal A06 is set up become Vrefb=1.9(V) of the output terminal A07. According to this setting out, the voltage per step becomes (4-1.9) / 255(V), and is set to about 8 (mV), a dynamic range spreads and the higher-precision amendment of it is attained.

[0025]Repeat Step S2 which is in this state and was performed previously - S4, namely, adjust the output from the output terminals A02 and A03, and black level correction (DC offset amendment) is performed (S7), The output from the output terminals A04 and A05 is adjusted, white level amendment (gain control) is performed (S8), the output from the output terminal A01 is adjusted, and gray balance amendment (Vref adjustment) is performed (S9). Thus, by assigning a D/A converter for every amendment, by the adjusting operation which could open the dynamic range further and was stabilized, high-precision amendment is attained and a high-definition read image can be obtained. Also in a natural monochrome case, it is applicable although explanation of this example explained by the case where three-line type color CCD series is used.

[0026]

[Effect of the Invention](1) When the picture signal from an image sensor is digitized according to this invention, the processing parameter (DC offset.) in the analog picture signal processing means formed in the preceding paragraph of the reference signal (conversion parameter) in an A/D converter, and the A/D converter By having controlled the dynamic range of the D/A converter which sets up a gain, and having made it possible to adjust a preset value with the greatest dynamic range, The accuracy of digital conversion and the accuracy of various level adjusting of a picture signal simultaneously performed by this adjustment are raised, and a high-definition read picture can be obtained by being stabilized.

[0027](2) . Based on the digital output which is outputted from an A/D converter in addition to the effect of the above (1), control the dynamic range of a D/A converter. That is, by feeding back the A/D conversion result of a picture signal and controlling the dynamic range of a D/A converter, Optimal range comprehension is performed automatically, the accuracy of digital conversion and the accuracy of various level adjusting of a picture signal simultaneously performed by this adjustment are raised further, and a high-definition read picture can be obtained by being stabilized. When materializing control of the dynamic range of a D/A converter, an easy means can realize by adjusting the preset value of the reference signal (reference signal) used for D/A conversion according to the digital output after the A/D conversion of the picture signal in an A/D converter.

[0028](3) In [in addition to the effect of the above (1) and (2)] a D/A converter, Further the reference signal (reference signal) used for D/A conversion by setting up and inputting the digital output after the A/D conversion of a picture signal as a variable value, It is possible to output the conversion parameter or processing parameter used for each output channel after analogue conversion as a preset value in an A/D converter and an analog signal processing circuit, respectively, So that gray balance amendment of a picture signal may be performed in an A/D converter, Since amendment of such a picture signal can make it simultaneous when it is made to perform black level correction of a picture signal, and/or white level amendment in an analog signal processing circuit and the picture signal from an image sensor is digitized, a high-definition read picture can be obtained by being stabilized.

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TECHNICAL FIELD

[Field of the Invention]In this invention, the level of the reference signal used for the analog processing of the picture signal output from a line image sensor and A/D conversion processing is adjusted more to details about the image reader which reads a manuscript by the scan of a line image sensor according to a sensor output.
Therefore, it is related with the image reader which raised the accuracy of the picture signal output after processing.

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PRIOR ART

[Description of the Prior Art]It is ********** about amendment of the shading compensation etc. which amend the luminous energy distribution of a light source, and the sensitivity distribution of CCD to the picture signal which performed the image input with the line image sensor (CCD) of the image reader, and was read in the former by CCD in a copying machine, a scanner, etc. Since these processings are usually performed in the stage which digitized after carrying out the A/D conversion of the analog output from CCD in the case of a digital machine, the fall of resolution is not avoided for a quantization error. Also when carrying out an A/D conversion, taking offset used as the factor which lowers resolution, and changing a profit into the optimal possible state and carrying out an A/D conversion, it is necessary to remove the influence of the ground of a manuscript and to make a picture output with the digital value of a high resolution (high gradation), in order to cope with such a thing.
[0003]one conventional example proposed as art to which the picture which should remove and read the influence of the ground of a manuscript is made to output with the digital value of a high resolution is because the reference voltage of an A/D converter is changed. When this changes fixed voltage and a programmed voltage for the reference voltage of an A/D converter with a switch and it reads only one manuscript, A switch chooses fixed voltage, and when reading the manuscript conveyed one by one by an automatic draft feeder in a read position, a switch chooses the variable voltage set up by analog circuitry composition, is changed according to a generating picture, and enables it to adjust image concentration automatically properly.
[0004]One example which will be accepted is what performs an automatic setup of the reference signal for A/D conversions by a different method from the above conventionally, The peak hold circuit which detects the peak value of the output from an A/D converter is provided, the reference signal for A/D conversions is controlled and the high-resolution digital output of the picture which should be read is secured so that the peak value detected by this circuit may serve as a full scale of an A/D conversion. Therefore, in this example, after processing the digital output from an A/D converter by a digital circuit system, the D/A converter was provided in the final stage, it changed into the analog value, and this is inputted into the A/D converter as a reference signal for A/D conversions. Operation of the A/D converter at the time of adjusting the reference signal of the A/D converter performed to this appearance and a D/A converter is explained more below at details.
[0005]Drawing 8 is a figure showing the outline composition of an A/D converter. A/D converter 41 like a graphic display The one analog input terminal Vin, The digital output terminals BIT0-BIT7 for two or more minutes (for example, 8 bits), It has terminal $Vref^+$ for maximums (the power supply voltage VCC is taken as the maximum), and terminal $Vref^-$ for minimums (ground voltage VSS is usually taken) as the clock terminal CLK which determines the timing of an A/D conversion, and a terminal which determines the reference voltage of the upper and lower sides for A/D conversions. Total of the digital output from A/D converter 41 : sigmaBITi, If it is decided by Vin, $Vref^+$, and $Vref^-$ and a full scale of a digital output is set to FS, it will be
$sigmaBITi=FSx(Vin-Vref^-)/(Vref^+-Vref^-)$.... (1)
If it carries out, and it is expressed and $Vref^-$ is made into a ground with resolution (i= 8) of 8

bits, since it will be $Vref^-$=0 and FS=255, the above-mentioned formula (1) is
sigmaBITi=255xVin/$Vref^+$.... (2)
It becomes. That is, total of a digital output is determined by the ratio of Vin and $Vref^+$.
reference voltage -- upper limit -- the digital output by Vin in that case if setting out of the pressure value of $Vref^+$ is lower than Vin -- a full scale -- 255 will be outputted, but to Vin, if too high, gradation will be made useless. Therefore, as for the value of $Vref^+$, it is desirable to set up become equal to the maximum which Vin can take. In order to set this up automatically, the analog value according to a peak value is set up as $Vref^+$ by performing the peak hold of the digital output of A/D converter 41, and inputting the held peak value into a D/A converter.
[0006]Drawing 9 is a figure showing the outline composition of a D/A converter. The input terminal Vreft in which D/A converter 51 leads to the power supply VCC like a graphic display. everything but the input terminal Vrefb connected with grand VSS -- serial-data input terminal DI, the shift clock input terminal CLK, LD input terminal, and two or more minutes -- for example, the analog output terminals A01-A08 of ** are formed by eight channels. Since part precision, temporality, environment, etc. may become a factor and dispersion may arise, the voltage VCC of constant value has been built over the terminal Vreft for maximums.
It is usually made into VCC=5(V).
The serial data whose data length is 12 bits are inputted into serial-data input terminal DI. As for 8 bits of low ranks of serial data, top 4 bits becomes address selections by the object for level setting of output voltage. The input signal from DI input terminal is inputted into 12 bit shift registers in the standup of the shift clock inputted from the shift clock input terminal CLK. If a High level is inputted into LD input terminal, the value of the data currently held at 12 bit-shift REJITA will be set in the register for an output. In the circuitry of this conventional example, by 5(V), supposing Vrefb is 0(V) in GND, Vref in the above-mentioned formula (2) will serve as 5(V) s, and as for Vin, Vreft which takes the fixed pressure value is digitized at a rate over 5(V)s. Therefore, the voltage per data 1 step becomes 5(mV) / 255 (mV), i.e., about 20.

[Translation done.]

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EFFECT OF THE INVENTION

[Effect of the Invention](1) When the picture signal from an image sensor is digitized according to this invention, the processing parameter (DC offset.) in the analog picture signal processing means formed in the preceding paragraph of the reference signal (conversion parameter) in an A/D converter, and the A/D converter By having controlled the dynamic range of the D/A converter which sets up a gain, and having made it possible to adjust a preset value with the greatest dynamic range, The accuracy of digital conversion and the accuracy of various level adjusting of a picture signal simultaneously performed by this adjustment are raised, and a high-definition read picture can be obtained by being stabilized.
[0027](2) . Based on the digital output which is outputted from an A/D converter in addition to the effect of the above (1), control the dynamic range of a D/A converter. That is, by feeding back the A/D conversion result of a picture signal and controlling the dynamic range of a D/A converter, Optimal range comprehension is performed automatically, the accuracy of digital conversion and the accuracy of various level adjusting of a picture signal simultaneously performed by this adjustment are raised further, and a high-definition read picture can be obtained by being stabilized. When materializing control of the dynamic range of a D/A converter, an easy means can realize by adjusting the preset value of the reference signal (reference signal) used for D/A conversion according to the digital output after the A/D conversion of the picture signal in an A/D converter.
[0028](3) In [in addition to the effect of the above (1) and (2)] a D/A converter, Further the reference signal (reference signal) used for D/A conversion by setting up and inputting the digital output after the A/D conversion of a picture signal as a variable value, It is possible to output the conversion parameter or processing parameter used for each output channel after analogue conversion as a preset value in an A/D converter and an analog signal processing circuit, respectively, So that gray balance amendment of a picture signal may be performed in an A/D converter, Since amendment of such a picture signal can make it simultaneous when it is made to perform black level correction of a picture signal, and/or white level amendment in an analog signal processing circuit and the picture signal from an image sensor is digitized, a high-definition read picture can be obtained by being stabilized.

[Translation done.]

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TECHNICAL PROBLEM

[Problem(s) to be Solved by the Invention]However, in adjustment of the above-mentioned reference voltage of an A/D converter, like the first example, when reference voltage is set up by the system of analog circuitry composition, a system is in instability, and it is **. For example, when the noise which has especially a constant period on a pulse when a noise mixes in a power supply mixes, a noise depressing effect with an amplifier will decrease remarkably, and a noise will mix also in an output. Since a peak hold or sample hold has determined the reference voltage level for A/D converters in the unstable state where ** which a noise will mix also according to ambient conditions, and such a noise can mix, it becomes a thing in which the stability of the whole system is also spoiled. Since the level fluctuation by temperature may arise, image deterioration will arise gradually over a long time. If the accuracy of amendment was also required and the reference signal Vref of the D/A converter was fixed to constant value (5(V)) in the second example when high definition was required, It becomes impossible for the dynamic range of a D/A converter to be insufficient, it cannot adjust to the value of a request of the reference voltage set as an A/D converter, and cannot meet the high-definition demand enough.

[0008]This invention was made in view of the problem of the above conventional technologies, and the purpose, When digitizing the analog picture signal from an image sensor, the D/A converter which sets up the reference signal (processing and conversion parameter) used for processing and conversion of a picture signal is made to adjust a preset value with the greatest dynamic range, It is in providing the reader which makes it possible to obtain a high-definition read picture by being stabilized by raising the accuracy of various level adjusting of a picture signal performed by raising the accuracy of the digital conversion of a picture signal, and adjusting processing and a conversion parameter simultaneously.

[Translation done.]

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MEANS

[Means for Solving the Problem]A picture signal processing means by which an invention of claim 1 processes and changes an analog picture signal with which it is outputted from an image sensor and this image sensor based on parameter value set as variable, In an image reader which it has, a control means which controls operation of this picture signal processing means said control means, A dynamic range is provided with a controllable D/A converter, and constitutes an image reader adjusting parameter value set up by this D/A converter in said picture signal processing means.
[0010]In the image reader according to claim 1, an invention of claim 2 said picture signal processing means, While having an A/D converter which carries out the A/D conversion of the analog picture signal outputted from said image sensor based on a reference signal value set as variable, A preset value of a reference signal in this A/D converter is adjusted by said D/A converter.
[0011]In the image reader according to claim 1 or 2, an invention of claim 3 said picture signal processing means, While having an analog signal processing circuit which processes an analog picture signal outputted from said image sensor based on a processing parameter set as variable, A preset value of a processing parameter in this analog signal processing circuit is adjusted by said D/A converter.
[0012]As for an invention of claim 4, in the image reader according to any one of claims 1 to 3, a dynamic range is controlled based on a digital output to which said D/A converter is outputted from said A/D converter.
[0013]An invention of claim 5 performs control of a dynamic range of said D/A converter by adjusting a preset value of a reference signal used for D/A conversion in the image reader according to any one of claims 1 to 4.
[0014]In the image reader according to any one of claims 2 to 5, an invention of claim 6 performs gray balance amendment of a picture signal, when said D/A converter adjusts a preset value of a reference signal in said A/D converter based on the output.
[0015]In the image reader according to any one of claims 3 to 6, an invention of claim 7 said D/A converter, By adjusting a preset value of a processing parameter in said analog signal processing circuit based on the output, black level correction of a picture signal and/or white level amendment are performed.
[0016]
[Embodiment of the Invention]It explains based on the example of the following shown with the drawing which attaches this invention. Drawing 1 is a figure showing the outline of the composition of the color copy reader which applied this invention. First, the entire configuration of this device is explained with reference to drawing 1. The contact glass 1 with which a device lays the manuscript 14, and the halogen lamp 2 for manuscript exposure, The 1st carriage 6 in which the 1st reflective mirror 3 was laid, and the 2nd carriage 7 in which the 2nd reflective mirror 4 and the 3rd reflective mirror 5 were laid, Three-line type color CCD series 9 which carries out photoelectric conversion of the picture in which image formation is carried out by the lens unit 8, It comprises the sensor board board 10, the CCD signal treating substrate 12 which performs various kinds of processings to a picture signal, the connecting cable 11, the white

reference board 15 for amending various kinds of distortion by a reading light study system etc., and the scanner body 13 that equips these. At the time of reading operation, with a stepping motor (not shown), it is moved in the direction of arrow A in a figure, and the 1st carriage 6 and the 2nd carriage 7 carry out vertical scanning of the manuscript surface on the contact glass 1, and read the whole manuscript surface.

[0017]Drawing 2 is a figure showing the acceptance surface of three-line type color CCD series 9. Reduced type CCD which coated the filter of each color of the decomposed colors R (red), G (green), and B (blue) as each line image sensor by the type which was able to be located in a line. As for R-CCD16, G-CCD17, and B-CCD18, the dot position of the scanning direction is the same the arrangement which shifted to the vertical scanning direction A the constant interval every. Therefore, since each color outputs have delay in the vertical scanning direction A, the amendment using a line memory is needed. Drawing 3 is a block diagram showing the circuitry of three-line type color CCD series 9. It has a register of two rows which R-CCD16, G-CCD17, and B-CCD18 divide the picture signal detected by the even number (EVEN) pixel and odd number (ODD) pixel in each light sensing portion, and holds each signal. The picture signal VRE, VRO, VGE, VGO, VBE, and VBO are independently outputted by driving a register synchronizing with (that is, on the whole, it has CCD registers 1-6) and a drive pulse.

[0018]Drawing 4 is a time chart which shows the correlation of the timing of various kinds of signals for driving CCD. The shift signal SH for transporting to a CCD register from a light sensing portion, and the transfer clock phi 1 for carrying out charge transfer of the inside of a CCD register and phi 2, A drive pulse generally comprises phiCLP for clamping pulse phiRS for resetting the output buffer in CCD, and the electric black level immediately after reset. Receiving light is continued during the period when a light sensing portion is from the shift signal SH to the following shift signal SH. This time is called storage time. The transfer clock phi 1 and phi 2 are the frequency which can transmit all the pixels of CCD in this storage time, and it becomes conditions that a transfer clock does not move during active period length in the shift signal SH. Vo shown in drawing 4 is a generating picture. Drawing 5 is a block diagram showing more in details the image processing circuit which it has in the signal processing substrate 12 in the color copy reader of drawing 1. The signal processing substrate 12 is equipped with the analog signal processing circuit 40, the A/D conversion circuit 41, the shading correction circuit 42, the correction circuit 43 between lines, the control circuit 44, and the oscillator 45.

[0019]Operation of an image processing circuit is mainly explained with reference to drawing 5. First, it is irradiated with a manuscript by the halogen lamp 2, and reduction image formation of the catoptric light from the manuscript 14 is carried out on three-line type color CCD line sensor 9 through the lens unit 8 through the 1st carriage 6 and the 2nd carriage 7, and it is read for every line. On the sensor board board 10 which receives the read picture signal, a picture signal is outputted to the CCD signal treating substrate 12 from three-line type color CCD line sensor 9 synchronizing with the drive pulse SH. This analog picture signal is inputted into the analog signal processing circuit 40 of the CCD signal treating substrate 12. By sampling a picture signal by a sample pulse, respectively, and holding it by a sample hold circuit (not shown), in the analog signal processing circuit 40, A picture signal is made into the continuous analog signal, the level of the dark output of CCD is detected in a black level correction circuit (not shown), the variation in a signal is amended on the basis of a black level, and the picture signal after amendment is outputted. In order that a picture signal may amend the real light volume decided by relation between CCD sensitivity and manuscript surface illumination, AGC (Auto Gain Control) is made.

[0020]The analog signal outputted from the analog signal processing circuit 40 is changed into a digital signal by the A/D conversion circuit 41. It is carried out by digital processing after the shading correction circuit 42 of the next step, and here, Based on the picture signal which read the catoptric light of the white reference board 15 irradiated by the halogen lamp 2 with three-line type color CCD line sensor 9, the luminous-intensity-distribution nonuniformity of the variation in the sensitivity of CCD or illuminating system is amended so that the level of predetermined concentration may be obtained. In the correction circuit 43 between lines, a gap of each line is amended using the memory for amendment between lines, and the delay produced

between R [of a vertical scanning direction], G, and B each line writing with 3line type as explained with reference to drawing 2 is outputted as a picture signal read in the same position. In the control circuit 44, the control signal which controls operation of each above-mentioned processing circuit 40, i.e., an analog signal processing circuit, the A/D conversion circuit 41, the shading correction circuit 42, and the correction circuit 43 between lines is generated. in addition -- being based on the clock from the oscillator 45 in that case -- a system -- the whole operation and the timing of a signal are adjusted.

[0021]In the CCD signal treating substrate 12, from three-line type color CCD line sensor 9 to R. G and B -- about each the two analog picture signals (ODD, EVEN) VRE, VRO, VGE, VGO, VBE, and VBO in the analog processing circuit 40, [amend and] It is necessary to change into a digital value by A/D converter 41 of the next step, it is necessary to perform initial setting so that reading operation of the scanner part which actually reads a manuscript can be performed, and control for it is performed. In this case, by A/D converter 41, gray balance amendment (Vref adjustment) is performed for ODD/EVEN difference amendment, black level correction (DC offset amendment), and white level amendment (gain control) in the analog signal processing circuit 40. In this invention, these amendments are performed based on the digital output value of A/D converter 41, and it is controlled by the analog value outputted from the D/A converter which considers this digital value as an input. He is trying to adjust the reference voltage in a D/A converter to the greatest dynamic range by feeding back the digital output of A/D converter 41. Feedback of the digital output value in this control is performed when CPU (not shown) of the control circuit 44 reads the data currently held with the digital value detection register of the shading correction circuit 42. The input to a D/A converter is performed via the control circuit 44 in the form of 12 bits (8 bits of data) serial data.

[0022]Next, the initialization action in each processing circuit by the composition of a control system and the control system which consist of the analog signal processing circuit 40 and A/D converter 41 which are controlled by a D/A converter and the D/A converter is explained in detail. Drawing 6 is a block diagram showing the composition of this control system. A control system consists of D/A converter 51 into which control data is inputted with a digital value, A/D converter 41 by which the analog output from D/A converter 51 is set up, and an output is controlled with the set-up value, and the analog signal processing circuit 40. Serial-data input terminal DI, the shift clock input terminal CLK, LD input terminal, and the analog output terminals A01-A08 for eight channels other than the input terminals Vreft and Vrefb of reference voltage with which D/A converter 51 can adjust voltage from the exterior are provided. The serial data whose data length is 12 bits are inputted into serial-data input terminal DI. As for 8 bits of low ranks of serial data, top 4 bits becomes address selections by the object for level setting of output voltage. The input signal from DI input terminal is inputted into 12 bit shift registers in the standup of the shift clock inputted from the shift clock input terminal CLK. If a High level is inputted into LD input terminal, the value of the data currently held at 12 bit-shift REJITA will be set in the register for an output. The output voltage Vout of D/A converter 51 will change by the reference voltage Vreft and Vrefb which can be adjusted from input data: <DATA> and the outside, and the relation becomes like the following formulas.

Vout=Vrefb+(Vreft-Vrefb) x<DATA>/255 [0023]Drawing 7 shows the flow chart of the initialization action of each processing circuit performed by the above-mentioned control system. With reference to drawing 7, an initialization action is explained below. It writes in addition by parenthesis writing into an explanatory note for reference of the step number of drawing 7. At the time of the start of initial setting, an initial value is set as the reference voltage Vreft and Vrefb of D/A converter 51 (S1). Here, it is considered as Vreft=5(V) and Vrefb=0(V). When taking the composition of drawing 6, this reference voltage is made possible by setting out by setting <DATA> =0 as the channel of the analog output terminal A06 at the channel of <DATA>=255 and A07. The voltage per step at this time becomes (5-0) / 255(V), and is set to about 20 (mV).

[0024]By adjusting the output from the output terminals A02 and A03, and setting that value as the analog signal processing circuit 40 on this condition, Black level correction (DC offset amendment) is performed (S2), the output from the output terminals A04 and A05 is adjusted,

and white level amendment (gain control) is performed with the value (S3). Gray balance amendment (Vref adjustment) is performed by adjusting the output from the output terminal A01, and setting the value as $Vref^+$ of A/D converter 41. Next, the maximum obtained as a procedure adjusted to the greatest dynamic range by A01-A05 which were set up with the input value <DATA>, The minimum is calculated, the value exceeding a little maximum is set as the output terminal A06 (Vreft), and a value somewhat smaller than the minimum is reset to the output terminal A07 (Vrefb) (S5). The maximum of <DATA> concerning setting out to A01-A05 here, for example 200 (about 3.92 (V)s), When the minimum is 100 (about 1.96 (V)s), Vreft=4.0(V) of the output terminal A06 is set up become Vrefb=1.9(V) of the output terminal A07. According to this setting out, the voltage per step becomes (4-1.9) / 255(V), and is set to about 8 (mV), a dynamic range spreads and the higher-precision amendment of it is attained.

[0025]Repeat Step S2 which is in this state and was performed previously - S4, namely, adjust the output from the output terminals A02 and A03, and black level correction (DC offset amendment) is performed (S7), The output from the output terminals A04 and A05 is adjusted, white level amendment (gain control) is performed (S8), the output from the output terminal A01 is adjusted, and gray balance amendment (Vref adjustment) is performed (S9). Thus, by assigning a D/A converter for every amendment, by the adjusting operation which could open the dynamic range further and was stabilized, high-precision amendment is attained and a high-definition read image can be obtained. Also in a natural monochrome case, it is applicable although explanation of this example explained by the case where three-line type color CCD series is used.

[Translation done.]

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DESCRIPTION OF DRAWINGS

[Brief Description of the Drawings]
[Drawing 1]It is a figure showing the outline of the composition of the color copy reader which applied this invention.
[Drawing 2]It is a figure showing the acceptance surface of three-line type color CCD series 9.
[Drawing 3]It is a block diagram showing the circuitry of three-line type color CCD series.
[Drawing 4]It is a time chart which shows the correlation of the timing of various kinds of signals for driving CCD.
[Drawing 5]It is a block diagram showing more in details the image processing circuit which it has in the signal processing substrate of the color copy reader of drawing 1.
[Drawing 6]It is a block diagram showing the composition of the analog signal processing circuit and A/D converter which are controlled by the D/A converter.
[Drawing 7]The flow chart of the initialization action of each processing circuit performed by the control system of drawing 6 is shown.
[Drawing 8]A reference signal is a figure showing the outline composition of the conventional A/D converter in which variable setting out is possible.
[Drawing 9]It is a figure showing the outline composition of the conventional D/A converter used for setting out of the reference signal of an A/D converter.
[Description of Notations]
9--3-line type color CCD series, 10 -- Sensor board board, 12 [-- An analog signal processing circuit and 41 / -- An A/D conversion circuit, 42 / -- A shading correction circuit, 43 / -- The correction circuit between lines, 44 / -- A control circuit, 45 / -- An oscillator, 51 / -- D/A conversion circuit (converter).] -- A CCD signal treating substrate, 14 -- A manuscript and 15 -- A white reference board, 40

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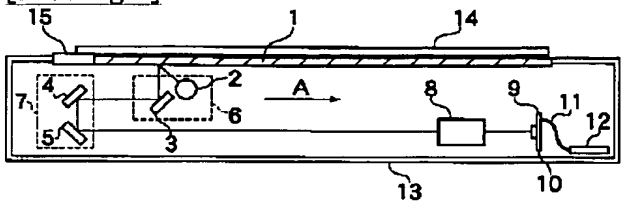
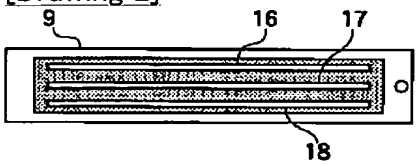
DRAWINGS

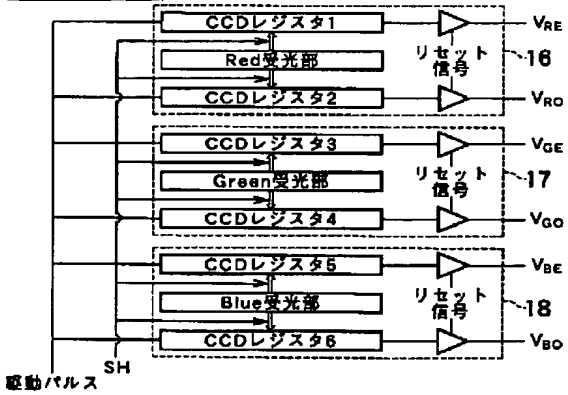
[Drawing 1]



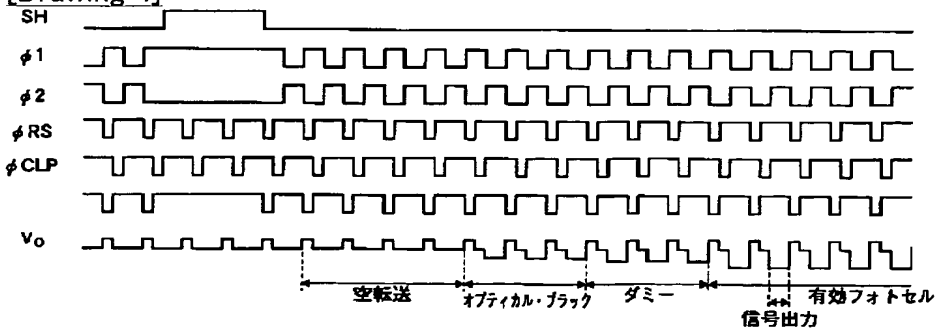
[Drawing 2]



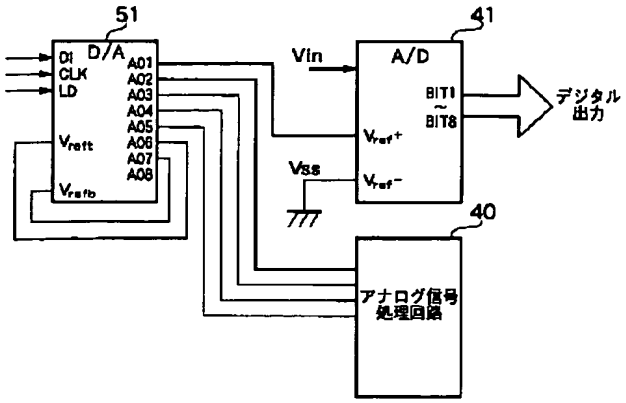
[Drawing 3]



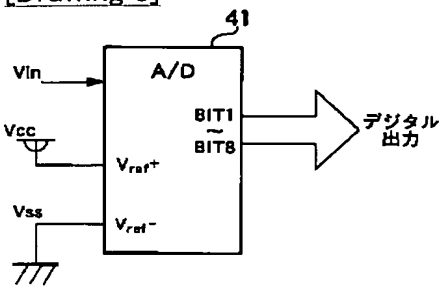
[Drawing 4]



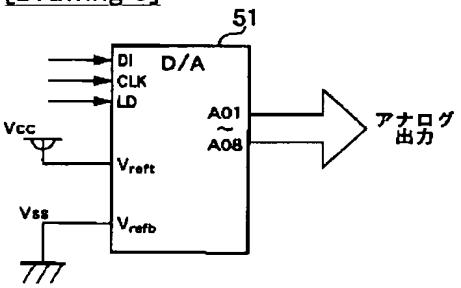
[Drawing 6]



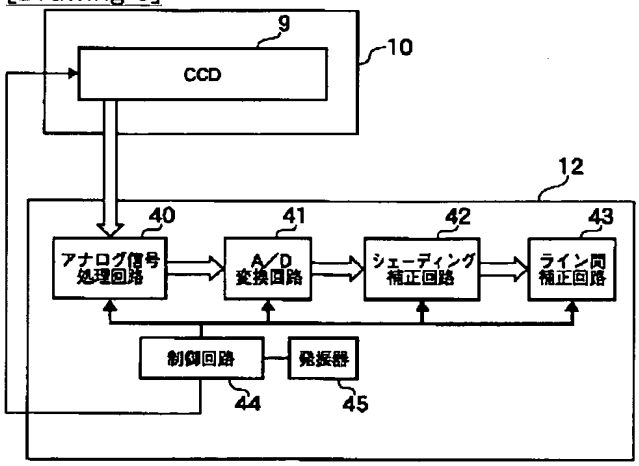
[Drawing 8]



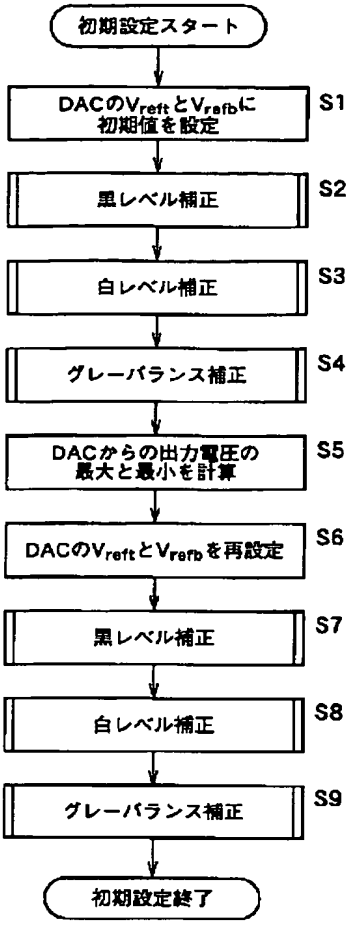
[Drawing 9]



[Drawing 5]



[Drawing 7]



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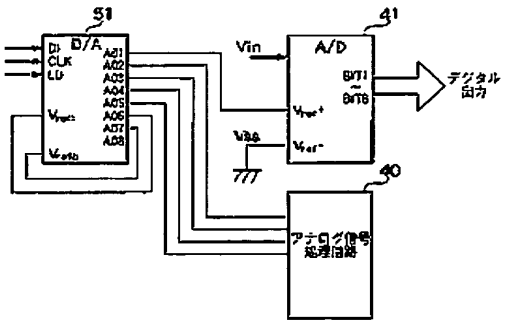
最終頁に続く

(54)【発明の名称】　画像読取装置

(57)【要約】
【課題】　イメージセンサからの画像信号をデジタル化する際、変換用の基準信号（変換パラメータ）を設定するＤ／Ａコンバータが最大のダイナミックレンジで設定値の調整を行うようにし、デジタル変換の精度と、この調整と同時に行う画像信号の各種レベル補正の精度を高め、高画質の読取画像を安定して得る。
【解決手段】　画像信号を処理するアナログ信号処理回路４０のオフセット、ゲイン調整とＡＤＣ４１の基準信号調整をＤＡＣ５１から出力される設定値により行う。ＡＤＣ４１のデジタル出力がフィードバックしＤＩとし入力されるＤＡＣ５１では、外部から電圧調整できる基準電圧Ｖreft、Ｖrefbに基づきＡ０１～Ａ０５から設定値を出力する。Ｖreft、Ｖrefbを初期値とし各種レベル補正をした場合に得られるＡＤＣ４１出力の最大値、最小値を基にＶreft、Ｖrefbを再設定し最大のダイナミックレンジで設定値の調整を行う。



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【特許請求の範囲】

【請求項１】　イメージセンサと、該イメージセンサから出力されるアナログ画像信号を、可変に設定されるパラメータ値に基づき処理・変換する画像信号処理手段と、該画像信号処理手段の動作を制御する制御手段とを有する画像読取装置において、前記制御手段は、ダイナミックレンジが制御可能なＤ／Ａコンバータを備え、該Ｄ／Ａコンバータにより前記画像信号処理手段において設定されるパラメータ値を調整することを特徴とする画像読取装置。

【請求項２】　前記画像信号処理手段は、前記イメージセンサから出力されるアナログ画像信号を、可変に設定されるリファレンス信号値に基づきＡ／Ｄ変換するＡ／Ｄコンバータを有するとともに、該Ａ／Ｄコンバータにおけるリファレンス信号の設定値が前記Ｄ／Ａコンバータにより調整されることを特徴とする請求項１記載の画像読取装置。

【請求項３】　前記画像信号処理手段は、前記イメージセンサから出力されるアナログ画像信号を、可変に設定される処理パラメータに基づき処理するアナログ信号処理回路を有するとともに、該アナログ信号処理回路における処理パラメータの設定値が前記Ｄ／Ａコンバータにより調整されることを特徴とする請求項１又は２記載の画像読取装置。

【請求項４】　前記Ｄ／Ａコンバータは、前記Ａ／Ｄコンバータから出力されるデジタル出力に基づいてダイナミックレンジが制御されることを特徴とする請求項１乃至３のいずれかに２記載の画像読取装置。

【請求項５】　前記Ｄ／Ａコンバータのダイナミックレンジの制御は、Ｄ／Ａ変換に用いるリファレンス信号の設定値を調整することにより行うことを特徴とする請求項１乃至４のいずれかに記載の画像読取装置。

【請求項６】　前記Ｄ／Ａコンバータは、その出力に基づき前記Ａ／Ｄコンバータにおけるリファレンス信号の設定値を調整することにより、画像信号のグレーバランス補正を行うことを特徴とする請求項２乃至５のいずれかに記載の画像読取装置。

【請求項７】　前記Ｄ／Ａコンバータは、その出力に基づき前記アナログ信号処理回路における処理パラメータの設定値を調整することにより、画像信号の黒レベル補正及び／又は白レベル補正を行うことを特徴とする請求項３乃至６のいずれかに記載の画像読取装置。

【発明の詳細な説明】

【０００１】

【発明の属する技術分野】本発明は、ラインイメージセンサの走査により原稿を読み取る画像読取装置に関し、より詳細には、ラインイメージセンサからの画像信号出力のアナログ処理及びＡ／Ｄ変換処理に用いる基準信号のレベルをセンサ出力に応じて調整することにより、処理後の画像信号出力の精度を上げるようにした画像読取

2

装置に関する。

【０００２】

【従来の技術】従来から、複写機、スキャナ等において、画像入力を画像読み取り装置のラインイメージセンサ（ＣＣＤ）により行い、ＣＣＤで読み取った画像信号に光源の光量分布、ＣＣＤの感度分布を補正するシェーディング補正、等の補正を施こしている。デジタル機の場合、通常、これらの処理はＣＣＤからのアナログ出力をＡ／Ｄ変換した後にデジタル化した段階で行われるため、量子化誤差のため分解能の低下が避けられない。こうしたことに対処するため、Ａ／Ｄ変換する時点で分解能を下げる要因となるオフセットを取り、利得をできるだけ最適な状態にし、又、Ａ／Ｄ変換する場合にも原稿の下地の影響を除去して画像を高分解能（高階調）のデジタル値で出力させる必要がある。

【０００３】原稿の下地の影響を除去して読み取るべき画像を高分解能のデジタル値で出力させる技術として提案された従来の１例は、Ａ／Ｄコンバータの基準電圧を変化させることによるものである。これは、Ａ／Ｄコンバータの基準電圧を固定電圧と設定電圧とをスイッチで切り替えるようにするもので、原稿を１枚だけ読み取る場合は、スイッチは固定電圧を選択し、自動原稿送り装置により順次読み取り位置に搬送されてくる原稿を読み取る場合は、スイッチはアナログ回路構成により設定される可変電圧を選択して画像出力に応じて変化させ画像濃度を適正に自動調整できるようにしている。

【０００４】従来のもう１つの例は、Ａ／Ｄ変換用の基準信号の自動設定を上記と異なる方法により行うもので、Ａ／Ｄコンバータからの出力のピーク値を検出するピークホールド回路を設け、この回路により検出されたピーク値がＡ／Ｄ変換のフルスケールとなるようにＡ／Ｄ変換用の基準信号を制御し、読み取るべき画像の高分解能デジタル出力を確保するものである。従って、この例では、Ａ／Ｄコンバータからのデジタル出力をデジタル回路系で処理した後に、最終段にＤ／Ａコンバータを設け、アナログ値に変えてこれをＡ／Ｄ変換用の基準信号としてＡ／Ｄコンバータへ入力している。この様に行われるＡ／Ｄコンバータの基準信号を調整する際のＡ／Ｄコンバータ及びＤ／Ａコンバータの動作を、以下に、より詳細に説明する。

【０００５】図８は、Ａ／Ｄコンバータの概略構成を示す図である。図示のように、Ａ／Ｄコンバータ４１は、１つのアナログ入力端子Ｖinと、複数分の、例えば８ビット分の、デジタル出力端子ＢｉＴ０～ＢｉＴ７と、Ａ／Ｄ変換のタイミングを決めるクロック端子ＣＬＫと、Ａ／Ｄ変換用の上下の基準電圧を決める端子として上限用端子Ｖref⁺（最大値として電源電圧ＶCCをとる）と、下限用端子Ｖref⁻（通常、グランド電圧ＶSSをとる）とを有する。Ａ／Ｄコンバータ４１からのデジタル出力の総和：ΣＢｉＴnは、ＶinとＶref⁺，Ｖref⁻に

よって決まり．デジタル出力のフルスケールをＦＳとす＊　＊れば．

$$\Sigma BiTi = FS \times (V_{in} - V_{ref}^{-}) / (V_{ref}^{+} - V_{ref}^{-}) \cdots\cdots (1)$$

として、表され．８ビットの分解能（ｉ＝８）で、Ｖref－をグランドとすれば、Ｖref－＝０、ＦＳ＝２５５であるから、上記式（１）は．

$$\Sigma BiT_1 = 255 \times V_{in} / V_{ref}^{+} \cdots\cdots (2)$$

となる。つまり．ＶinとＶref＋の比率によりデジタル出力の総和が決定される。基準高圧上限値なるＶref＋の電圧値の設定が、Ｖinより低いと．その場合のＶinによるデジタル出力はフルスケールなる２５５を出力してしまうことになり、かといって、Ｖinに対して高すぎると階調を無駄にしてしまう。従って．Ｖref＋の値は．Ｖinのとり得る最大値に等しくなるように設定するのが望ましい。これを自動で設定するために、Ａ／Ｄコンバータ４１のデジタル出力のピークホールドを行い．保持されたピーク値をＤ／Ａコンバータに入力することによりピーク値に応じたアナログ値をＶref＋として設定する。

【０００６】図９は、Ｄ／Ａコンバータの概略構成を示す図である。図示のように．Ｄ／Ａコンバータ５１は、高源ＶＣＣにつながる入力端子Ｖrefｔ．グランドＶＳＳにつながる入力端子Ｖrefbの他に、シリアルデータ入力端子ＤＩ．シフトクロック入力端子ＣＬＫ．ＬＤ入力端子および．複数分．例えば８チャネル分．のアナログ出力端子Ａ０１～Ａ０８が設けられている。上限用端子Ｖrefｔには．部品精度．経時．環境等が要因となってばらつきが生じることがあるために一定値の電圧ＶＣＣがかかっており．それは．通常ＶＣＣ＝５（Ｖ）とされている。シリアルデータ入力端子ＤＩには、データ長が１２ビットのシリアルデータが入力される。シリアルデータの下位８ビットは出力電圧のレベル設定用で上位４ビットがアドレス選択用となる。シフトクロック入力端子ＣＬＫから入力されるシフトクロックの立ち上がりでＤＩ入力端子からの入力信号が１２ビットシフトレジスタに入力される。ＬＤ入力端子にHighレベルが入力されると．１２ビットシフトレジタに保持されているデータの値が出力用レジスタにセットされる。この従来例の回路構成において．固定された電圧値をとるＶrefｔが５（Ｖ）で、ＶrefbがＧＮＤで０（Ｖ）であるとすると．上記式（２）におけるＶrefは５（Ｖ）となり．Ｖinは５（Ｖ）に対する割合でデジタル化される。従って、データ１ステップあたりの電圧は、５（mV）／２５５、即ち約２０（mV）となる。

【０００７】

【発明が解決しようとする課題】しかしながら．上記したＡ／Ｄコンバータの基準電圧の調整において．第一の例のように、アナログ回路構成の系で基準高圧を設定している場合、系が不安定になりやい。例えば、電源にノイズが侵入した場合、特にパルス上の一定周期を持つノイズが侵入した場合には．増幅器とのノイズ抑圧効果が著しく減少し．出力にもノイズが侵入することになる。また．周囲条件によってもノイズが混入することになり．このようなノイズが混入し得るような不安定な状態でピークホールド又はサンプルホールドにてＡ／Ｄ変換器用の基準高圧値を決定しているため．系全体の安定性も損なわれる物となる。さらには、温度によるレベル変動が生じ得るため、長時間にわたって次第に画像劣化が生じることになる。また．第二の例では、高画質が要求されてくると補正の精度も要求され．Ｄ／Ａコンバータの基準信号Ｖrefを一定値（５（Ｖ））に固定したのでは．Ｄ／Ａコンバータのダイナミックレンジが足りなくなり．Ａ／Ｄ変換器に設定される基準電圧を所望の値に調整することができず、高画質の要求に十分応えることができない。

【０００８】本発明は、上記のような従来技術の問題点に鑑みなされたもので、その目的は．イメージセンサからのアナログ画像信号をデジタル化する際に、画像信号の処理・変換に用いる基準信号（処理・変換パラメータ）を設定するＤ／Ａコンバータが最大のダイナミックレンジで設定値の調整を行うようにし．画像信号のデジタル変換の精度を高め、また同時に．処理・変換パラメータを調整することにより行われる画像信号の各種レベル補正の精度を高めることにより高画質の読取画像を安定して得ることを可能とする読取装置を提供することにある。

【０００９】

【課題を解決するための手段】請求項１の発明は．イメージセンサと．該イメージセンサから出力されるアナログ画像信号を．可変に設定されるパラメータ値に基づき処理・変換する画像信号処理手段と．該画像信号処理手段の動作を制御する制御手段とを有する画像読取装置において、前記制御手段は．ダイナミックレンジが制御可能なＤ／Ａコンバータを備え、該Ｄ／Ａコンバータにより前記画像信号処理手段において設定されるパラメータ値を調整することを特徴とする画像読取装置を構成する。

【００１０】請求項２の発明は、請求項１記載の画像読取装置において．前記画像信号処理手段は、前記イメージセンサから出力されるアナログ画像信号を、可変に設定されるリファレンス信号値に基づきＡ／Ｄ変換するＡ／Ｄコンバータを有するとともに、該Ａ／Ｄコンバータにおけるリファレンス信号の設定値が前記Ｄ／Ａコンバータにより調整されることを特徴とするものである。

【００１１】請求項３の発明は、請求項１又は２記載の画像読取装置において、前記画像信号処理手段は．前記イメージセンサから出力されるアナログ画像信号を、可

変に設定される処理パラメータに基づき処理するアナログ信号処理回路を有するとともに、該アナログ信号処理回路における処理パラメータの設定値が前記Ｄ／Ａコンバータにより調整されることを特徴とするものである。

【００１２】請求項４の発明は、請求項１乃至３のいずれかに記載の画像読取装置において、前記Ｄ／Ａコンバータは、前記Ａ／Ｄコンバータから出力されるデジタル出力に基づいてダイナミックレンジが制御されることを特徴とするものである。

【００１３】請求項５の発明は、請求項１乃至４のいずれかに記載の画像読取装置において、前記Ｄ／Ａコンバータのダイナミックレンジの制御は、Ｄ／Ａ変換に用いるリファレンス信号の設定値を調整することにより行うことを特徴とするものである。

【００１４】請求項６の発明は、請求項２乃至５のいずれかに記載の画像読取装置において、前記Ｄ／Ａコンバータは、その出力に基づき前記Ａ／Ｄコンバータにおけるリファレンス信号の設定値を調整することにより、画像信号のグレーバランス補正を行うことを特徴とするものである。

【００１５】請求項７の発明は、請求項３乃至６のいずれかに記載の画像読取装置において、前記Ｄ／Ａコンバータは、その出力に基づき前記アナログ信号処理回路における処理パラメータの設定値を調整することにより、画像信号の黒レベル補正及び／又は白レベル補正を行うことを特徴とするものである。

【００１６】

【発明の実施の形態】本発明を添付する図面とともに示す以下の実施例に基づき説明する。図１は、本発明を適用したカラー原稿読取装置の構成の概要を示す図である。先ず、図１を参照して本装置の全体構成を説明する。装置は、原稿１４を載置するコンタクトガラス１と、原稿露光用のハロゲンランプ２と、第１反射ミラー３を載置した第１キャリッジ６と、第２反射ミラー４及び第３反射ミラー５を載置した第２キャリッジ７と、レンズユニット８によって結像される画像を光電変換する３ライン型カラーＣＣＤイメージセンサ９と、センサボード基板１０と、画像信号に各種の処理を施すＣＣＤ信号処理基板１２と、接続ケーブル１１と、読み取り光学系等による各種の歪みを補正するための白基準板１５と、これらを装備するスキャナ本体１３から構成される。読み取り動作時には、第１キャリッジ６及び第２キャリッジ７はステッピングモータ（図示せず）によって図中の矢印Ａ方向に移動され、コンタクトガラス１上の原稿面を副走査し原稿全面の読み取りを行う。

【００１７】図２は、３ライン型カラーＣＣＤイメージセンサ９の受光面を示す図である。各ラインイメージセンサとして分解色Ｒ（レッド）、Ｇ（グリーン）、Ｂ（ブルー）の各色のフィルタをコーティングした縮小型ＣＣＤをならべたタイプで、Ｒ－ＣＣＤ１６，Ｇ－ＣＣＤ１７，Ｂ－ＣＣＤ１８は主走査方向のドット位置が同じく、副走査方向Ａに一定間隔ずつずれた配置になっている。従って各色出力が副走査方向Ａにディレイをもつのでラインメモリを使った補正が必要となる。図３は、３ライン型カラーＣＣＤイメージセンサ９の回路構成を示すブロック図である。Ｒ－ＣＣＤ１６，Ｇ－ＣＣＤ１７，Ｂ－ＣＣＤ１８はそれぞれの受光部における偶数（ＥＶＥＮ）画素と奇数（ＯＤＤ）画素により検出された画像信号を分けて各々の信号を保持する２列のレジスタを持ち（即ち、全体ではＣＣＤレジスタ１～６を有する）、駆動パルスに同期してレジスタを駆動することにより、画像信号ＶＲＥ、ＶＲＯ、ＶＧＥ、ＶＧＯ、ＶＢＥ、ＶＢＯを独立に出力する。

【００１８】図４はＣＣＤを駆動するための各種の信号のタイミングの相互関係を示すタイムチャートである。受光部からＣＣＤレジスタに移送するためのシフト信号ＳＨと、ＣＣＤレジスタ内を高速転送するための転送クロックφ１、φ２と、ＣＣＤ内の出力バッファをリセットするためのパルスφＲＳと、リセット直後の電気的な黒レベルをクランプするためのφＣＬＰから駆動パルスは一般的に構成される。受光部はシフト信号ＳＨから次のシフト信号ＳＨまでの期間、受光し続ける。この時間を蓄積時間という。転送クロックφ１，φ２は、この蓄積時間内にＣＣＤの全画素を転送できる周波数で、シフト信号ＳＨがアクティブ期間中に転送クロックが動かないことが条件となる。図４に示すＶｏは、画像出力である。図５は図１のカラー原稿読取装置における信号処理基板１２に有する画像処理回路をより詳細に示すブロック図である。信号処理基板１２には、アナログ信号処理回路４０と、Ａ／Ｄ変換回路４１と、シェーディング補正回路４２と、ライン間補正回路４３と、制御回路４４と、発振器４５を備える。

【００１９】画像処理回路の動作を主に図５を参照して説明する。まず、原稿はハロゲンランプ２により照射され、原稿１４からの反射光は第１キャリッジ６、第２キャリッジ７を通じてレンズユニット８を通り３ライン型カラーＣＣＤラインセンサ９上に縮小結像し、１ライン毎に読み取られる。読み取られた画像信号を受け取るセンサボード基板１０上では、３ライン型カラーＣＣＤラインセンサ９から駆動パルスＳＨに同期して、画像信号がＣＣＤ信号処理基板１２に出力される。このアナログ画像信号は、ＣＣＤ信号処理基板１２のアナログ信号処理回路４０に入力される。アナログ信号処理回路４０では、サンプルホールド回路（図示せず）によって画像信号をそれぞれサンプルパルスによりサンプリングし保持することによって、画像信号を連続したアナログ信号にし、黒レベル補正回路（図示せず）においてＣＣＤの暗出力のレベルを検出し、黒レベルを基準として信号のバラツキを補正し、補正後の画像信号を出力する。また、画像信号は、ＣＣＤ感度と原稿面照度との関係で決まる

実質光量を補正するためにＡＧＣ（Auto Gain Control）がなされる。

【００２０】アナログ信号処理回路４０から出力されたアナログ信号は、Ａ／Ｄ変換回路４１によりデジタル信号に変換される。次段のシェーディング補正回路４２以降はデジタル処理が行われ、ここでは、ハロゲンランプ２により照射された白基準板１５の反射光を３ライン型カラーＣＣＤラインセンサ９で読み取った画像信号に基づいて、所定の濃度のレベルが得られるように、ＣＣＤの感度のバラツキや照射系の配光ムラを補正する。ライン間補正回路４３では、図２を参照して説明したように３ライン型としたために副走査方向のＲ、Ｇ、Ｂ各ライン間に生じるディレイをライン間補正用のメモリを用いて各ラインのずれを補正して、同一位置で読取った画像信号として出力する。制御回路４４では、上記した各処理回路、即ちアナログ信号処理回路４０、Ａ／Ｄ変換回路４１、シェーディング補正回路４２及びライン間補正回路４３の動作を制御する制御信号を生成している。なお、その際に発振器４５からのクロックに基づいて系全体の動作や信号のタイミングを調整する。

【００２１】ＣＣＤ信号処理基板１２では、３ライン型カラーＣＣＤラインセンサ９からＲ、Ｇ、Ｂそれぞれについて２系統（ODD, EVEN）のアナログ画像信号V_{RE}、V_{RO}、V_{GE}、V_{GO}、V_{BE}、V_{BO}をアナログ処理回路４０で補正して、次段のＡ／Ｄコンバータ４１でデジタル値に変換し、原稿を実際に読み取るスキャナ部の読み取り動作ができるように初期設定を行う必要があり、そのための制御を行う。この場合、アナログ信号処理回路４０で、ODD／EVEN差補正、黒レベル補正（ＤＣオフセット補正）、白レベル補正（ゲインコントロール）を、Ａ／Ｄコンバータ４１ではグレーバランス補正（Ｖref調整）を行う。本発明において、これらの補正はＡ／Ｄコンバータ４１のデジタル出力値に基づいて行われ、このデジタル値を入力とするＤ／Ａコンバータから出力されるアナログ値により制御される。また、Ｄ／Ａコンバータにおける基準電圧を、Ａ／Ｄコンバータ４１のデジタル出力をフィードバックすることにより最大のダイナミックレンジに調整するようにしている。このコントロールにおけるデジタル出力値のフィードバックは、シェーディング補正回路４２のデジタル値検出レジスタで保持されているデータを制御回路４４のＣＰＵ（図示せず）が読み込むことにより行われる。Ｄ／Ａコンバータへの入力は、１２ビット（データ８ビット）のシリアルデータの形式で制御回路４４を介して行われる。

【００２２】次に、Ｄ／ＡコンバータとＤ／Ａコンバータによりコントロールされるアナログ信号処理回路４０及びＡ／Ｄコンバータ４１よりなる制御系の構成及び制御系による各処理回路における初期設定動作を詳細に説明する。図６は、この制御系の構成を示すブロック図である。制御系は、デジタル値で制御データが入力されるＤ／Ａコンバータ５１と、Ｄ／Ａコンバータ５１からのアナログ出力が設定され、設定された値により出力がコントロールされるＡ／Ｄコンバータ４１及びアナログ信号処理回路４０とからなる。Ｄ／Ａコンバータ５１は、外部から電圧が調整できる基準電圧の入力端子Ｖreft、Ｖrefbの他に、シリアルデータ入力端子ＤＩ、シフトクロック入力端子ＣＬＫ、ＬＤ入力端子及び、８チャネル分のアナログ出力端子Ａ０１～Ａ０８が設けられている。シリアルデータ入力端子ＤＩには、データ長が１２ビットのシリアルデータが入力される。シリアルデータの下位８ビットは出力電圧のレベル設定用で上位４ビットがアドレス選択用となる。シフトクロック入力端子ＣＬＫから入力されるシフトクロックの立ち上がりでＤＩ入力端子からの入力信号が１２ビットシフトレジスタに入力される。ＬＤ入力端子にHighレベルが入力されると、１２ビットシフトレジスタに保持されているデータの値が出力用レジスタにセットされる。Ｄ／Ａコンバータ５１の出力電圧Ｖoutは、入力データ：（DATA）と、外部から調整できる基準電圧Ｖreftと Ｖrefbにより変わることになり、その関係は以下の式のようになる。

$$V_{out} = V_{refb} + (V_{reft} - V_{refb}) \times (DATA) / 255$$

【００２３】図７は、上記の制御系により行われる各処理回路の初期設定動作のフローチャートを示す。図７を参照して、初期設定動作を以下に説明する。なお、説明文中に括弧書きで図７のステップ番号を参照のために付記する。初期設定のスタート時に、Ｄ／Ａコンバータ５１の基準電圧Ｖreftと Ｖrefbに初期値を設定する（Ｓ１）。ここでは、Ｖreft＝５（Ｖ）、Ｖrefb＝０（Ｖ）とする。図６の構成をとる場合、アナログ出力端子Ａ０６のチャネルに（DATA）＝２５５、Ａ０７のチャネルに（DATA）＝０を設定することにより、この基準電圧が設定可能になされる。このときの１ステップあたりの電圧は、（５－０）／２５５（Ｖ）となり、約２０（mV）となる。

【００２４】この条件で、出力端子Ａ０２・Ａ０３からの出力を調整してアナログ信号処理回路４０にその値を設定することにより、黒レベル補正（DCオフセット補正）を行い（Ｓ２）、出力端子Ａ０４・Ａ０５からの出力を調整してその値で白レベル補正（ゲインコントロール）を行う（Ｓ３）。また、出力端子Ａ０１からの出力を調整してその値をＡ／Ｄコンバータ４１のＶref＋に設定することにより、グレーバランス補正（Ｖref調整）を行う。次に、最大のダイナミックレンジに調整する手順として、入力値（DATA）によって設定されたＡ０１～Ａ０５によって得られる最大値、最小値を求め、最大値を少し越える値を出力端子Ａ０６（Ｖreft）に設定し、最小値より少し小さい値を出力端子Ａ０７（Ｖrefb）に再設定する（Ｓ５）。ここで、例えば、Ａ０１～Ａ０５までの設定に係わる（DATA）の最大値が２００

（約３．９２（V））．最小値が１００（約１．９６（V））である場合に．出力端子Ａ０６のVreft＝４．０（V）．を出力端子Ａ０７のVrefb＝１．９（V）となるように設定する。この設定によると．１ステップあたりの電圧は、（４－１．９）／２５５（V）となり、約８（mV）となりダイナミックレンジが広がり、より精度の高い補正が可能となる。

【００２５】この状態で．また、先に行ったステップＳ２～Ｓ４を繰り返し、即ち出力端子Ａ０２・Ａ０３からの出力を調整して黒レベル補正（ＤＣオフセット補正）を行い（Ｓ７）．出力端子Ａ０４・Ａ０５からの出力を調整して白レベル補正（ゲインコントロール）を行い（Ｓ８）、出力端子Ａ０１からの出力を調整してグレーバランス補正（Vref調整）を行う（Ｓ９）。このように．Ｄ／Ａコンバータを各補正ごとに割り当てることにより．一層ダイナミックレンジを広げることができ、また．安定した調整動作によって、精度の高い補正が可能となり、高画質の読み取り画像を得ることができる。なお．本実施例の説明では．３ライン型カラーＣＣＤイメージセンサを用いた場合で説明したが．もちろん白黒の場合にも適用できる。

【００２６】

【発明の効果】（１）　本発明によると、イメージセンサからの画像信号をデジタル化する際．Ａ／Ｄコンバータにおけるリファレンス信号（変換パラメータ）及びＡ／Ｄコンバータの前段に設けたアナログ画像信号処理手段における処理パラメータ（ＤＣオフセット、ゲイン）の設定を行うＤ／Ａコンバータのダイナミックレンジを制御するようにし、最大のダイナミックレンジで設定値の調整を行うことを可能としたことにより、デジタル変換の精度と、この調整によって同時に行われる画像信号の各種レベル補正の精度を高め、高画質の読取画像を安定して得ることができる。

【００２７】（２）　上記（１）の効果に加えて．Ａ／Ｄコンバータから出力されるデジタル出力に基づいてＤ／Ａコンバータのダイナミックレンジを制御する．つまり．画像信号のＡ／Ｄ変換結果をフィードバックしＤ／Ａコンバータのダイナミックレンジを制御することにより．最適なレンジ調整を自動的に行い．デジタル変換の精度と、この調整によって同時に行われる画像信号の各種レベル補正の精度をさらに高め、高画質の読取画像を安定して得ることができる。また、Ｄ／Ａコンバータのダイナミックレンジの制御を具体化する場合に．Ａ／Ｄコンバータにおける画像信号のＡ／Ｄ変換後のデジタル出力に従いＤ／Ａ変換に用いるリファレンス信号（基準信号）の設定値を調整することにより簡単な手段で実現できる。

【００２８】（３）上記（１）、（２）の効果に加えて．Ｄ／Ａコンバータにおいて、Ｄ／Ａ変換に用いるリファレンス信号（基準信号）を、さらには画像信号のＡ／Ｄ変換後のデジタル出力を、可変値として設定・入力することにより．アナログ変換後の各出力チャンネルにＡ／Ｄコンバータ、アナログ信号処理回路においてそれぞれ設定値として用いる変換パラメータあるいは処理パラメータを出力することが可能で、Ａ／Ｄコンバータでは画像信号のグレーバランス補正を行うように．また、アナログ信号処理回路では画像信号の黒レベル補正及び／又は白レベル補正を行うようにし．イメージセンサからの画像信号をデジタル化する際にこうした画像信号の補正が同時にすることができるので．高画質の読取画像を安定して得ることができる。

【図面の簡単な説明】

【図１】本発明を適用したカラー原稿読取装置の構成の概要を示す図である。

【図２】３ライン型カラーＣＣＤイメージセンサ９の受光面を示す図である。

【図３】３ライン型カラーＣＣＤイメージセンサの回路構成を示すブロック図である。

【図４】ＣＣＤを駆動するための各種の信号のタイミングの相互関係を示すタイムチャートである。

【図５】図１のカラー原稿読取装置の信号処理基板に有する画像処理回路をより詳細に示すブロック図である。

【図６】Ｄ／Ａコンバータによりコントロールされるアナログ信号処理回路及びＡ／Ｄコンバータの構成を示すブロック図である。

【図７】図６の制御系により行われる各処理回路の初期設定動作のフローチャートを示す。

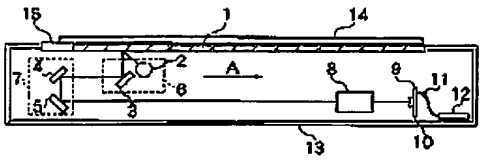
【図８】基準信号が可変設定可能な従来のＡ／Ｄコンバータの概略構成を示す図である。

【図９】Ａ／Ｄコンバータの基準信号の設定に用いる従来のＤ／Ａコンバータの概略構成を示す図である。

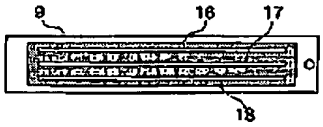
【符号の説明】

９…３ライン型カラーＣＣＤイメージセンサ、１０…センサボード基板．　１２…ＣＣＤ信号処理基板、１４…原稿、　１５…白基準板．４０…アナログ信号処理回路、　４１…Ａ／Ｄ変換回路．４２…シェーディング補正回路．４３…ライン間補正回路、４４…制御回路．　４５…発振器．５１…Ｄ／Ａ変換回路（コンバータ）。

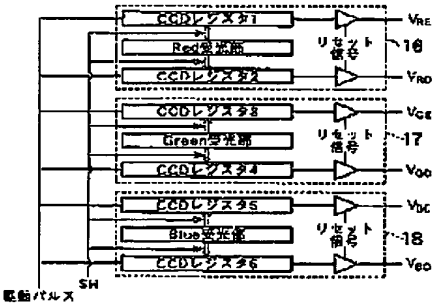
【図１】



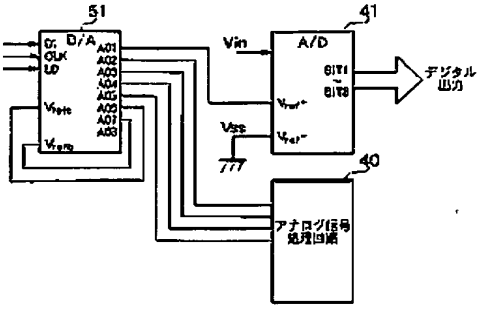
【図２】



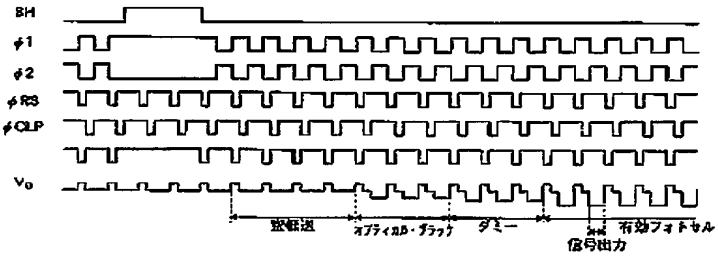
【図３】



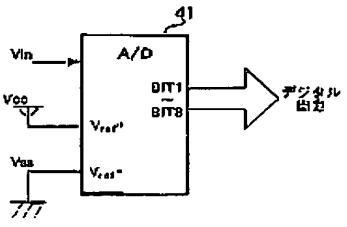
【図６】



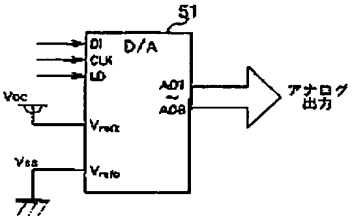
【図４】



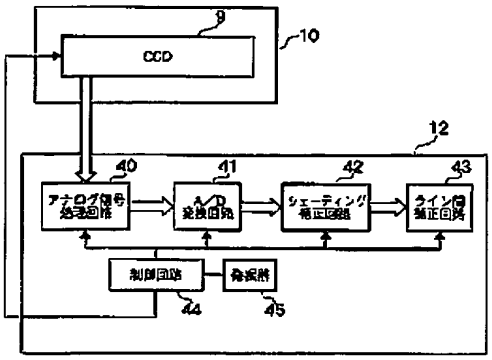
【図８】



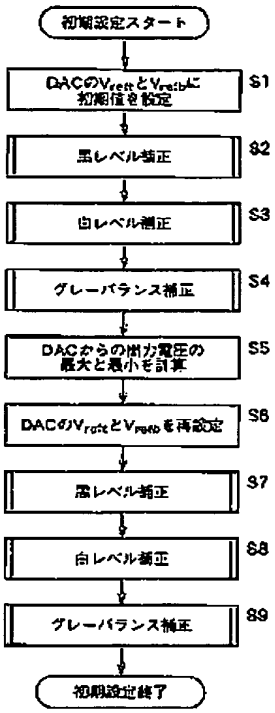
【図９】



【図５】



【図７】



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